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EXAMINER	
STOREY, WILLIAM C	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/806,910	GRAF ET AL.	
	Examiner	Art Unit	
	WILLIAM C. STOREY	2625	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 March 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,4-11,14-18,20,23-28 and 31-43* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,4-11,14-18,20,23-28 and 31-43* is/are rejected.

7)☒ Claim(s) *15, 17, 28, 37, & 42* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The specification is objected to as failing to provide proper antecedent basis for the claimed subject matter. See 37 CFR 1.75(d)(1) and MPEP § 608.01(o). Correction of the following is required: Claims 11 & 28 recites that the print controller acts on the valid or invalid first serial data stream. Support for this addition cannot be found at least where the applicant claimed support for the amendments may be found (pg. 11 of applicant's remarks). Providing a proposition that that the print host "can" (or is able to) take corrective or preventative action, is not the same as showing the print host as actually acting on the valid or invalid data.

2. The specification is objected to as failing to provide proper antecedent basis for the claimed subject matter. See 37 CFR 1.75(d)(1) and MPEP § 608.01(o). Correction of the following is required: Claim 11 recites that the print host sends a serial command comprising a request for a reference data stream at a reference location within the data stream. Support for this addition cannot be found at least where the applicant claimed support for the amendments may be found (pg. 11 of applicant's remarks).

Claim Objections

3. Claim 17 is objected to because of the following informalities: Claim 17 refers to a dependence from claim 13. Claim 13 has been cancelled. The examiner will assume that the applicant intended claim 17 to depend from claim 11. Appropriate correction is required.

4. A claim is objected to as failing to provide proper antecedent basis for the claimed subject matter. See 37 CFR 1.75(d)(1) and MPEP § 608.01(o). Correction of the following is required: Claim 17 discloses forming the reference data stream with a data stream independent of the first serial data stream. However, claim 11, which from above claim 17 has been determined to be dependent from, states adding the reference data stream into the data stream...thereby forming a first serial data stream. Thus, the first serial data stream comprises the reference data stream, and thus, it is impossible for the reference data stream to be formed with a data stream independent of the first serial data stream. The examiner will assume the applicant to mean the data stream instead of the first serial data stream in claim 17.

5. A claim is objected to as failing to provide proper antecedent basis for the claimed subject matter. See 37 CFR 1.75(d)(1) and MPEP § 608.01(o). Correction of the following is required: Claim 28 refers to "the serial data stream." However, there is "a first serial data stream" claimed. The examiner assumes the applicant to intend "the serial data stream" to mean "the first serial data stream."

6. Claim 37 is objected to as failing to provide proper antecedent basis for the claimed subject matter. See 37 CFR 1.75(d)(1) and MPEP § 608.01(o). Correction of the following is required: Claim 37 refers to "the first data stream." However, no first data stream has been defined in the dependency structure associated with this claim. The examiner will assume the applicant to mean "the first serial data stream."

7. The amendments to the claims filed on 3/17/2008 does not comply with the requirements of 37 CFR 1.121(c) because changes were made which were not properly

identified: Claim 15 as amended has omitted "cyclic code, arithmetic code, Berger code, Hamming code, horizontal parity code" with respect to the original claim 15, yet proper declaration of this amendment was not made. Claim 42 has been amended, yet claims to be the "original" claim. As the intent of the applicant can be reasonably inferred by comparison with other amended claims, the examiner will only object to the claims as of now. Please correct these deficiencies with the next correspondence so that noncompliance will not be necessitated.

Claim Rejections - 35 USC § 112

8. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

9. Claims 11 & 28 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Claims 11 & 28 recites that the print controller acts on the valid or invalid first serial data stream. Support for this addition cannot be found at least where the applicant claimed support for the amendments may be found (pg. 11 of applicant's remarks). Providing a proposition that that the print host "can" (or is able to) take corrective or preventative action, is not the same as showing the print host as actually acting on the valid or invalid data.

10. Claim 11 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Claim 11 recites that the print host sends a serial command comprising a request for a reference data stream at a reference location within the data stream. Support for this addition cannot be found at least where the applicant claimed support for the amendments may be found (pg. 11 of applicant's remarks).

11. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

12. Claim 7 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claim 7 recites "the method of claim 5, wherein the start bits, the sync bits and the stop bits have at least two bits of different voltage values." The method of claim 5 refers to at least one of a plurality of start bits, a plurality of sync bits, [or] a plurality of stop bits. Claim 7, as is, stands indefinite as is and it is unclear as to whether one of the start bits, sync bits, or stop bits is to have at least two bits of different voltage values, whether all of the listed bits together comprise at least two bits of different voltage values, or whether each and all of the start bits, sync bits, and stop bits are to have at least two bits of different voltage values. Please specify.

Claim Rejections - 35 USC § 103

13. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

14. Claims 1, 4-6, 28, & 32-37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Skene et al. (US Patent 6616260), hereinafter referred to as Skene, in view of Hepworth et al. (US 3975712), hereinafter referred to as Hepworth.

Regarding claim 1, Skene discloses communication between a printhead and a controller, which reads on claimed print host, print host coupled to a print head, communicating a first data stream between the printer host and the print head; as disclosed in column 4, lines 11-20 and figure 1. Skene discloses setting parity bits in data that are to be communicated in order to detect possible errors, which reads on claimed inserting a reference data stream into the first data stream; as disclosed at column 7, lines 55-58. Skene discloses checking the parity bit that was included in the data stream to check whether or not the data has an error, which reads on claimed validating the first data stream based on the reference data stream; as disclosed at column 8, lines 41-45, for example.

Skene discloses individual lines for individual bits, as disclosed in column 3, lines 66-67 and column 4 lines 1-10. However, Skene does not distinctly disclose wherein the first data stream comprises a serial data stream and inserting a reference data

stream into the first serial data stream.

In a similar field of endeavor, Hepworth discloses a communication interface adaptor. In addition, Hepworth discloses data being converted from a parallel transmittal form into a serial transmittal form, which reads on claimed wherein the first data stream comprises a serial data stream; as disclosed at column 3, lines 26-31. Hepworth discloses inserting a reference data stream into a serial data stream (col. 7, lines 23-30 disclose serializing the data and then adding or inserting bits, like parity bits (reference data stream)).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Skene by specifically providing wherein the first data stream comprises a serial data stream and inserting a reference data stream into the first serial data stream, as taught by Hepworth, for the purpose of reducing package size.

However, Skene fails to disclose wherein the act of communicating the first data stream further comprises the act of synchronously communicating the first data stream.

In a similar field of endeavor, Hepworth discloses a communication interface adaptor. In addition, Hepworth discloses data being transmitted through shift register based on a clock signal, which reads on claimed wherein the act of communicating the first data stream further comprises the act of synchronously communicating the first data stream; as disclosed at column 3, lines 26-31.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Skene by specifically providing wherein the act

of communicating the first data stream further comprises the act of synchronously communicating the first data stream, as taught by Hepworth, for the purpose of reducing latency.

Regarding claim 4, Skene discloses everything as applied above for claim 1. Skene discloses memory integrated with the inkjet printhead assembly, as disclosed in column 3, lines 58-59. Bits, which read on claimed data, are located in the memory, as disclosed in column 3, lines 48-49. A controller causes the reading of data from the memory as disclosed above, causing the data to be sent and thus, received. The parity bit, which reads on claimed reference data stream, is inserted into the list of bits being communicated in the claimed first data stream, as disclosed above. This reads on claimed transmitting a print head data stream comprising the first data stream and the reference data stream from the print head; and receiving the print head data stream at the printer host.

Regarding claim 5, Skene discloses everything as applied above for claim 1. The parity bit, which reads on claimed reference data stream, is inserted into the list of bits being communicated in the claimed first data stream, as disclosed above. However, Skene fails to disclose wherein the act of inserting the reference data stream further comprises the act of adding to the first serial data stream at least one of a plurality of start bits, a plurality of sync bits, a plurality of stop bits, and at least one error detection bit.

In a similar field of endeavor, Hepworth discloses a communication interface adaptor. In addition, Hepworth discloses, after the data is serialized for transmission,

inserting a start bit and a trailing stop bit or bits and that a parity may be included, which reads on claimed wherein the act of inserting the reference data stream further comprises the act of adding to the first serial data stream at least one of a plurality of start bits, a plurality of sync bits, a plurality of stop bits, and at least one error detection bit, as disclosed in column 7, lines 23-30.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Skene by specifically providing wherein the act of inserting the reference data stream further comprises the act of adding to the first serial data stream at least one of a plurality of start bits, a plurality of sync bits, a plurality of stop bits, and at least one error detection bit, as taught by Hepworth, for the purpose of adding definition to serial data transmission that enables better control and robustness.

Regarding claim 6, Skene and Hepworth disclosed everything as applied above for claim 5. Skene and Hepworth both disclosed the use of a parity code above, which reads on claimed wherein the error detection bit comprises at least one of a parity check code, residue code, "m" of "n" code, duplication code, cyclic code, arithmetic code, Berger code, Hamming code, horizontal parity code, or vertical parity code.

Regarding claim 28, Skene discloses communication between a printhead and a controller, which reads on claimed print controller adapted to be coupled to the print head and print head configured to transmit a data stream; as disclosed in column 4, lines 11-20 and figure 1. Skene discloses setting parity bits, which reads on claimed reference data stream; in data that are to be communicated in order to detect possible

errors, as disclosed at column 7, lines 55-58. Skene discloses checking the parity bit that was included in the data stream to check whether or not the data has an error, which reads on claimed validating the received data stream when the validating data stream comprises a valid data stream pattern; as disclosed at column 8, lines 41-45, for example. In order to validate the transmitted stream, which reads on claimed transmitted and received data stream; based on the parity code, which reads on claimed validating data stream; that parity code bit must be found, which means it has have been searched for. Skene discloses the parity code being checked against different odd or even patterns (valid data stream pattern) or else the stream will not be valid, which reads on claimed validating data stream comprises a valid data stream; as disclosed at column 3, lines 48-49 and column 7, lines 55-67 & column 8, lines 1-8. In addition, Skene discloses acting on the valid or invalid first serial data stream (Col. 40-50 discloses an example of where the analysis of the parity bit provides justification of an error, and then correcting a value accordingly).

However, Skene did not distinctly disclose the data stream in serial form, inserting the reference data stream into a first serial data stream at a reference location; synchronously transmitting and receiving the first serial data stream from the print head, another means for searching for a validating data stream from the transmitted first serial data stream and another means for validating the received first serial data stream when the validating data stream comprises a valid data pattern.

In a similar field of endeavor, Hepworth discloses a communication interface adaptor. Hepworth discloses data being converted from a parallel transmittal form into

a serial transmittal form, which reads on claimed first serial data stream; as disclosed at column 3, lines 26-31. In addition, Hepworth discloses, after the data is serialized for transmission, inserting a start bit and a trailing stop bit or bits and that a parity may be included, as disclosed in column 7, lines 23-30. Col. 7, lines 23-30 disclose that two stop bits are trailing and that the parity is inserted between the last data bit and the first stop bit, thus reading on claimed insert a reference data stream into the first serial data stream at a reference location. In addition, Hepworth discloses that the serial communication synchronously clocked for transmission (synchronously transmit the first serial data stream), col. 3, lines 24-52. Hepworth discloses searching for a validating data stream at the reference location from the transmitted first serial data stream: the nature of stop bits and their being able to be interpreted as signaling a "stop," makes it inherent that they be searched out in order to correspond with a stop. In addition, col. 7, lines 58-67 & col. 8, lines 1-6 disclose checking for errors based off the reference bits that had been placed at their respective reference positions. A status register is set based on errors, which correspond to the reference bits. In addition, the parity bit is stripped from data being transferred to receiver data register. Therefore, the reference bits must have been searched for in order for these actions to occur. No errors means that the data stream is thus, valid. When the parallel/serial communication link would be between the print head and print host, then the first serial data stream would be received from the print head by the print controller.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Skene by specifically providing the data stream

in serial form inserting the reference data stream into a first serial data stream at a reference location; synchronously transmitting and receiving the first serial data stream from the print head another means for searching for a validating data stream from the transmitted first serial data stream and another means for validating the received first serial data stream when the validating data stream comprises a valid data pattern, as taught by Hepworth, for the purpose of reducing latency, better control, and allowing for a more robust system.

Regarding claim 32, the claim inherits everything as applied above for claim 28. It was disclosed previously how a reference data stream may be inserted in the first serial data stream. A box may be drawn around anything. Thus, the "print head" may also have incorporated with its box the adapter that allows for insertion of bits taught by Hepworth, just as the "print head" may also have a memory incorporated within, etc. Thus, the "print head" would insert the reference data stream into the first serial data stream.

Regarding claim 33, the claim inherits everything as applied above for claim 32. Stop, start, and parity (error detection) bits have already been disclosed as able to be added to the first serial data stream.

Regarding claim 34, claim 34 is rejected based on reasoning supplied above for claim 6.

Regarding claim 35, claim 35 is rejected based on reasoning supplied above for claim 16. Skene discloses the controller comparing the parity code with the pattern it should match to, which reads on claimed wherein the print controller compares the

reference pattern with the valid data pattern (odd or even parity); as disclosed at column 8, lines 36-37. In addition, Hepworth provided means at the receiving end of the transmission to check the parity, start, and stop bit reference data stream pattern (placement, even or odd parity) against what is known to be valid in order to determine errors. A box may be drawn around anything. The "print controller" may also have incorporated with its box the adapter that allows for checking for errors taught by Hepworth. Thus, the "print controller" would perform the comparison.

Regarding claim 36, claim 36 is rejected based on reasoning supplied above for claim 9. A box may be drawn around anything. Thus, the "print head" may also have incorporated with its box the adapter that allows for insertion of bits taught by Hepworth, just as the "print head" may also have a memory incorporated within, etc. Thus, the "print head" would form the reference data stream.

Regarding claim 37, claim 37 is rejected based on reasoning supplied above for claim 8. A box may be drawn around anything. Thus, the "print head" may also have incorporated with its box the adapter that allows for insertion of bits taught by Hepworth, just as the "print head" may also have a memory incorporated within, etc. Thus, the "print head" would form the reference data stream.

15. Claims 7-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Skene in view of Hepworth and further in view of Ono et al. (US 6943911), hereinafter referred to as Ono.

Regarding claim 7, Skene and Hepworth disclose everything as applied above for claim 5. However, Skene and Hepworth fail to disclose wherein the start bits, the

sync bits and the stop bits have at least two bits of different voltage values.

In a similar field of endeavor, Ono discloses a driving control apparatus and driving control method. In addition, Ono discloses a start bit constituted by two bits consisting of an H level and an L level, which reads on claimed at least one of a plurality of start bits, a plurality of sync bits, a plurality of stop bits, and thus wherein the start bits, the sync bits and the stop bits have at least two bits of different voltage values; as disclosed at column 5, line 67 and column 6, lines 1-2. H and L read on two different voltage values.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Skene by specifically providing wherein the start bits, the sync bits and the stop bits have at least two bits of different voltage values, as taught by Ono, for the purpose of giving a graphical break between the start of data transmission.

Regarding claim 8, Skene discloses everything as applied above for claim 1. However, Skene fails to disclose forming the reference stream with a plurality of bits independent of the first serial data stream.

In a similar field of endeavor, Ono discloses a driving control apparatus and driving control method. In addition, Ono discloses inserting start bits, which reads on claimed reference data; constituted by an H and an L level before the data being transmitted for effect (claimed first serial data stream), as disclosed at column 5, line 67 and column 6, lines 1-2 and 8-9. Because the start bits will always be comprised of an H level and an L level, this reads on claimed forming the reference stream with a

plurality of bits independent of the first data stream.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Skene by specifically providing forming the reference stream with a plurality of bits independent of the first data stream, as taught by Ono, for the purpose of signaling the start of the data being transmitted for effect.

It was discussed previously how the first data stream may be a first serial data stream. However, Skene and Ono did not distinctly disclose wherein the act of forming the reference data stream with a plurality of bits independent of the first serial data stream.

In a similar field of endeavor, Hepworth discloses a communication interface adaptor. In addition, Hepworth discloses, after the data is serialized for transmission, inserting a start bit and a trailing stop bit or bits and that a parity may be included, as disclosed in column 7, lines 23-30. This shows that bits, such as the aforementioned bits (which may act as reference bits) may be inserted into the first serial data stream.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Skene and Ono by specifically providing wherein the act of forming the reference data stream with a plurality of bits independent of the first serial data stream, as taught by Hepworth, for the purpose of adding definition to serial data transmission that enables better control and robustness to serial data.

Regarding claim 9, Skene discloses everything as applied above for claim 1. However, Skene fails to disclose forming the reference data stream with a non-uniform bit pattern.

In a similar field of endeavor, Ono discloses a driving control apparatus and driving control method. In addition, Ono discloses inserting a start bit, which reads on claimed reference data; constituted by an H and an L level before the data being transmitted for effect (claimed first serial data stream), as disclosed at column 5, line 67 and column 6, lines 1-2 and 8-9. Because the start bit is composed of two different levels, this reads on claimed forming the reference stream with a non-uniform bit pattern.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Skene by specifically providing forming the reference stream with a non-uniform bit pattern, as taught by Ono, for the purpose of giving a graphical break between the start of data transmission.

It was discussed previously how the first data stream may be a first serial data stream. However, Skene and Ono did not distinctly disclose forming the reference stream with a non-uniform bit pattern.

In a similar field of endeavor, Hepworth discloses a communication interface adaptor. In addition, Hepworth discloses, after the data is serialized for transmission, inserting a start bit and a trailing stop bit or bits and that a parity may be included, as disclosed in column 7, lines 23-30. This shows that bits, such as the aforementioned bits (which may act as reference bits) may be inserted into the first serial data stream.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Skene and Ono by specifically providing forming the reference stream with a non-uniform bit pattern, as taught by Hepworth, for the

purpose of adding definition to serial data transmission that enables better control and robustness to serial data.

16. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Skene in view of Hepworth as applied to claim 1 above, and further in view of Bullock et al. (US 5835817), hereinafter referred to as Bullock.

Regarding claim 10, Skene discloses everything as applied above in claim 1. Skene discloses memory integrated with the inkjet printhead assembly, as disclosed in column 3, lines 58-59. Bits excluding a parity bit, which read on claimed first data stream, are located in the memory, as disclosed in column 3, lines 48-49. A controller causes the reading of data from the memory as disclosed above. This reads on claimed retrieving the first data stream stored in a print head memory.

Skene discloses individual lines for individual bits, as disclosed in column 3, lines 66-67 and column 4 lines 1-10. However, Skene fails to disclose wherein the first data stream comprises a serial data stream.

In a similar field of endeavor, Hepworth discloses a communication interface adaptor. In addition, Hepworth discloses data being converted from a parallel transmittal form into a serial transmittal form, which reads on claimed wherein the first data stream comprises a serial data stream; as disclosed at column 3, lines 26-31.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Skene by specifically providing wherein the first data stream comprises a serial data stream, as taught by Hepworth, for the purpose of reducing package size.

The combination disclosed above provides for practical serial use of the interaction between print head memory and a print host. However, Skene did not distinctly disclose having a first serial data stream stored in a print memory.

In a similar field of endeavor, Bullock discloses serial memory for an ink cartridge. In addition, Bullock discloses having a first serial data stream stored in a print memory (figs. 4-5, col. 6, lines 15-19 disclose a serial memory chip (attached to an ink cartridge (60)) that enables input output of data over a single access wire. col. 6, lines 60-67 disclose parameters being stored in the memory and having the changed parameters being made available to a microprocessor. Col. 4, lines 52-55 disclose the memory being connected to the control computer for reading and writing actions between the two. Col. 4, lines 27-32 discloses protocol for transmitting and receiving (read/write) from the memory chip that enable bit-by-bit transfers, the ability to control insertion of start and stop bits (various length pulses which evidence the beginning of a read/write action) and overall serial input/output communication from the serial memory. All of this proves that it would have been well known to one of ordinary skill in the art at the time the invention was made to provide having a first serial data stream, (i.e. a serial number (col. 56-62)) stored in print head memory that may communicate a stream of data back and forth with a print host for the purpose of reducing the amount of interconnects and/or other adaptive circuitry.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Skene by specifically providing having a first

serial data stream stored in a print memory, as taught by Bullock, for the purpose of reducing the amount of interconnects and/or other adaptive circuitry.

Skene has provided the use of error-checking by the insertion of reference data into the data transmitted between a print head memory and controller. However, Bullock did not distinctly disclose wherein the act of inserting a reference data stream comprising a parity bit as discussed by Skene and having the serial transmission synchronized to a clock. Bullock has shown the capability of setting reference bits, such as a start and stop bits, discussed previously.

In a similar field of endeavor, Hepworth discloses a communication interface adaptor. In addition, Hepworth discloses, after the data is serialized for transmission, inserting a start bit and a trailing stop bit or bits and that a parity may be included, as disclosed in column 7, lines 23-30. In addition, Hepworth discloses that the serial communication synchronously clocked for transmission, col. 3, lines 24-52. Although Hepworth discloses shifting parallel data to serial data, the disclosure above provides for shifting out serial data at the beginning of transmission and shifting in serial data at the end of the synchronous transmission. Therefore, the examiner maintains that it would be obvious to one of ordinary skill in the art to provide for clocking serial data by shifts at both the input and output at the beginning and end of a transmission.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Bullock by specifically providing inserting a reference data stream comprising a parity bit and having transmission synchronized by a clock, as taught by Hepworth, for the purpose of adding definition to serial data

transmission that enables better control and robustness.

17. Claim 11 & 14-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bullock in view of Hepworth and Skene.

Regarding claim 11, Bullock discloses receiving a serial command (Col. 4, lines 27-32 discloses overall serial input/output communication from the serial memory) at the print head (figs. 4-5, col. 6, lines 15-19 disclose a serial memory chip (attached to an ink cartridge (60). The ink cartridge may read on claimed print head.) from the printer host (control computer may read on claimed printer host. Col. 4, lines 52-62 disclose that reading and writing may occur between the control computer and the memory. For example, in order to retrieve a serial number stored in the memory chip located at the ink cartridge, the computer would read the data, thus, reading on claimed receiving a serial command at the print head from the printer host.), the serial command comprising a request for a data stream (for example, request for a serial number); and retrieving the data stream from a print head memory (it is inherent that when the control computer reads, for example, a serial number from the memory, that a data stream would be retrieved from the print head memory).

Bullock has shown the capability of setting reference bits, such as a start and stop bits, as disclosed at col. 4, lines 27-32 (various length pulses which evidence the beginning of a read/write action). However, Bullock did not distinctly disclose wherein the reference data stream comprises a bit width of at least two adjacent bits, adding the reference data stream into the data stream at the reference location, thereby forming a first serial data stream; synchronously receiving the first serial data stream at the printer

host from the print head, and searching for the reference data stream at the reference location within the received first serial data stream.

In a similar field of endeavor, Hepworth discloses a communication interface adaptor. In addition, Hepworth discloses, after the data is serialized for transmission, inserting a start bit and a trailing stop bit or bits and that a parity may be included, as disclosed in column 7, lines 23-30. Col. 7, lines 23-30 disclose that two stop bits are trailing and that the parity is inserted between the last data bit and the first stop bit, thus reading on claimed adding the reference data stream into the data stream at the reference location. In addition, the two stop bits and the parity are adjacent and comprise a bit width of at least two adjacent bits. The addition of the reference data stream thereby forms a "first serial data stream" in conjunction with the data being sent. In addition, Hepworth discloses that the serial communication synchronously clocked for transmission, col. 3, lines 24-52. Although Hepworth discloses shifting parallel data to serial data, the disclosure above provides for shifting out serial data at the beginning of transmission and shifting in serial data at the end of the synchronous transmission. Therefore, the examiner maintains that it would be obvious to one of ordinary skill in the art to provide for clocking serial data by shifts at both the input and output at the beginning and end of a transmission. Thereby, there would be synchronous reception of the first serial data stream at the printer host from the print head. Hepworth discloses searching for the reference data stream at the reference location within the received first serial data stream: the nature of stop bits and their being able to be interpreted as signaling a “stop," makes it inherent that they be searched out in order to correspond

with a stop. In addition, col. 7, lines 58-67 & col. 8, lines 1-6 disclose checking for errors based off the reference bits that had been placed at their respective reference positions. A status register is set based on errors, which correspond to the reference bits. In addition, the parity bit is stripped from data being transferred to receiver data register. Therefore, the reference bits must have been searched for in order for these actions to occur.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Bullock by specifically providing wherein the reference data stream comprises a bit width of at least two adjacent bits, adding the reference data stream into the data stream at the reference location, thereby forming a first serial data stream; synchronously receiving the first serial data stream at the printer host from the print head, and searching for the reference data stream at the reference location within the received first serial data stream, as taught by Hepworth, for the purpose of reducing latency, better control, and allowing for a more robust system.

However, Bullock did not distinctly disclose a request for a reference data stream at a reference location within the data stream, searching for the reference data stream at the reference location within the received first serial data stream; validating the received first serial data stream when the received first serial data stream comprises the reference data stream at the reference location; and acting on the valid or invalid first serial data stream. In addition, Skene provides additional motivation for the addition of error-correction in a printing system.

In a similar field of endeavor, Skene discloses robust bit scheme for a memory of a replaceable printer component. In addition, Skene discloses a request for a reference data stream at a reference location within the data stream (col. 2, lines 5-10 disclose a first data item and a first parity read from the memory. It is inherent that there was some sort of request for the parity bit to be sent (request for reference data stream within the data stream (stream of data that is sent)). (Even though the invention of Skene discloses separate communication lines for data and parity, serial and parallel communication are both well known to those of ordinary skill in the art and the parallel data could be sent serially. Hepworth (col. 3, lines 24-52) shows a method for converting parallel to serial, for example.) Fig. 3 discloses the parity being in a specific reference location in order to determine if there was error, as is well known to those of ordinary skill in the art. Therefore, it is inherent in this system that the addition of the parity reference be at a specific reference location.) searching for the reference data stream at the reference location within the received first serial data stream (As disclosed earlier, the parity bit occupies a specific location. Col. 35-50 discloses the controller examining the parity bit to determine if there was an error in the data bit field (data stream with parity). In order to examine the parity bit, the bit would have had to have been searched for and found.); validating the received first serial data stream when the received first serial data stream comprises the reference data stream at the reference location (Fig. 3, fig. 5a-5b show the parity bit in a particular reference position. Col. 8, lines 35-50 disclose determining whether or not an error has occurred. If no error is determined to have occurred, then the first serial data stream would be validated.); and

acting on the valid or invalid first serial data stream (Col. 40-50 discloses an example of where the analysis of the parity bit provides justification of an error, and then correcting a value accordingly). Though Skene may provide some data in parallel format, Hepworth has shown communicating the same data serially. In addition, it is well known to communicate both serial and parallel ways.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Bullock by specifically providing a request for a reference data stream at a reference location within the data stream, searching for the reference data stream at the reference location within the received first serial data stream; validating the received first serial data stream when the received first serial data stream comprises the reference data stream at the reference location; and acting on the valid or invalid first serial data stream, as taught by Skene, for the purpose of providing the idea of error checking and correction that leads to a more robust system of transmission between print head memory and controller.

Regarding claim 14, the claim inherits everything as applied above for claim 11. It was disclosed previously adding start, stop, and parity (at least one error detection bit) to the first serial data stream.

Regarding claim 15, the claim inherits everything as applied above for claim 14. The previously-disclosed parity bit reads on claimed wherein the at least one error detection bit comprises a parity check code, residue code, "m" of "n" code, duplication code, or vertical parity code.

18. Claims 17-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bullock in view of Hepworth and Skene as applied above for claim 11, and further in view of Ono.

Regarding claim 17, the claim is rejected based upon similar reasoning as applied above for claim 8. In addition, claim 17 inherits everything as applied for claim 11.

Regarding claim 18, the claim is rejected based upon similar reasoning as applied above for claim 9. In addition, claim 18 inherits everything as applied for claim 11.

19. Claim 20 & 23-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Skene in view of Hepworth and further in view of Gibson et al. (US6161616), hereinafter referred to as Gibson.

Regarding claim 20, Skene discloses communication between an inkjet printhead and a controller, which reads on claimed host, print head communication link coupling the print head and the host, and configured to communicate a first data stream between the print head and the host; as disclosed in column 4, lines 11-20 and figure 1. Skene discloses setting parity bits, which reads on claimed insert a reference data stream; in data that are to be communicated, which reads on claimed first data stream; in order to detect possible errors, which reads on claimed error detection; as disclosed at column 7, lines 55-58. Skene discloses memory integrated with the inkjet printhead assembly, which reads on claimed data stream register coupled to the print head; as disclosed in column 3, lines 58-59. Bits, which read on claimed data stream, are located in the

memory and a parity bit is set based on a pattern in order to check for errors, as disclosed in column 3, lines 48-49 and column 7, lines 55-67 & column 8, lines 1-8. Skene discloses the controller checking the parity bit that was included in the data stream to check whether or not the data has an error, which reads on claimed data validating controller coupled to the host, and configured to validate the first data stream based on the reference stream; as disclosed at column 8, lines 35-36 & 41-45, for example.

However, Skene did not distinctly disclose the data being transmitted in a serial form, wherein the first serial data stream is synchronously sequenced at a frequency of the clocking control signal, inserting a reference data stream into the first serial data stream at a reference location.

In a similar field of endeavor, Hepworth discloses a communication interface adapter. Hepworth discloses data being converted from a parallel transmittal form into a serial transmittal form, which reads on claimed first serial data stream; as disclosed at column 3, lines 26-31. Skene had disclosed using a parity reference in order to validate data streams. Hepworth allows the addition of parity, start, and stop reference bits into a serial data stream which may be used to communicated between a print head and a host (col. 7, lines 23-30 disclose serializing the data and then adding or inserting bits, like parity bits (reference data stream)). In addition, Hepworth shows that a reference data stream may be inserted at a reference location. Col. 7, lines 23-30 disclose the start bit leading, the stop bit or bits trailing, and parity occurring between the last data bit and first stop bit. Hepworth discloses data being transmitted through shift register

based on a clock signal from a clock, which reads on claimed wherein the first serial data stream is synchronously sequenced at a frequency of the clock control signal (clock signal); as disclosed at column 3, lines 26-33 and claim 3. Hepworth also supplies means to check the parity and for errors in order to determine the validity of the transmitted data (col. 7, 58-67 & col. 8, lines 1-6).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Skene by specifically providing the data being transmitted in a serial form, wherein the first serial data stream is synchronously sequenced at a frequency of the clocking control signal, inserting a reference data stream into the first serial data stream at a reference location, as taught by Hepworth, for the purpose of for the purpose of reducing latency, better control, and allowing for a more robust system.

However, Skene and Hepworth did not distinctly disclose a clocking control signal generated by the host. However, Hepworth disclosed a clock (generated clocking control signal), and it would be pretty obvious to place that or have it come from within a titular box called "the host." Clock signal generation has been taught and placing it at one position over another does not really provide any patentable distinction in this case. However, in order to provide further motivation for such a placement, the following is provided.

In a similar field of endeavor, Gibson discloses parallel/serial conversion from print head memory. In addition, Gibson discloses Fig. 2, col. 7, lines 36-38 disclose

clock signals being able to come from printer electronics 22 (which may read on claimed host and contains a controller).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Skene and Hepworth by specifically providing a clocking control signal generated by the host, as taught by Gibson, for the purpose of keeping the majority of control electronics together for organizational purposes.

Regarding claim 23, the claim is rejected based upon similar reasoning provided for claim 20.

Regarding claim 24, Skene and Hepworth disclosed everything as applied above for claim 23. Skene and Hepworth both disclosed the use of a parity code above, which reads on claimed wherein the at least one error detection bit comprises at least one of a parity check code, residue code, "m" of "n" code, duplication code, cyclic code, arithmetic code, Berger code, Hamming code, horizontal parity code, or vertical parity code.

20. Claim 25 is rejected under 35 U.S.C. 103(a) as being unpatentable over Skene in view of Hepworth and Gibson as applied above for claim 20 and further in view of Barbour et al. (US 6476928), hereinafter referred to as Barbour.

Regarding claim 25, Skene discloses everything as applied above for claim 20. The examiner maintains that it was well known in the art to provide a print head retrieving a first data stream from a print head memory, as taught by Barbour.

In a similar field of endeavor, Barbour discloses a system and method for controlling internal operations of a processor of an inkjet printhead. In addition, Barbour

discloses a processor and various controllers within a printhead that may communicate with a memory in the printhead and Barbour discloses the memory holding sensor readings that the processor uses to make decisions, as disclosed at column 5, lines 17-20 and column 8, lines 40-50 and 57-59, which reads on claimed print head receives a first data stream from a print head memory. Thus it can be seen reasonable to one of ordinary skill in the art for the processor to take readings from the memory rather than directly from the sensors. Barbour also discloses the processor communicating with a main memory in a bi-directional manner, as disclosed at lines 40-45.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Skene by specifically providing a print head retrieving a first data stream from a print head memory, as taught by Barbour, for the purpose of processing the data before sending it out to the main controller.

The amendment specifying a data stream to be serial should not make a difference. Serial and parallel communication are both well known. Serial/parallel conversion has been taught to be well known.

21. Claims 26-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Skene in view of Hepworth and Gibson as applied above for claim 20 and further in view of Ono.

Regarding claim 26, Skene discloses everything as applied above for claim 20. However, Skene fails to disclose forming the reference stream with a non-uniform bit pattern.

In a similar field of endeavor, Ono discloses a driving control apparatus and

driving control method. In addition, Ono discloses inserting a start bit, which reads on claimed reference data; constituted by an H and an L level before the data being transmitted for effect (claimed first data stream), as disclosed at column 5, line 67 and column 6, lines 1-2 and 8-9. Because the start bit is composed of two different levels, this reads on claimed forming the reference stream with a non-uniform bit pattern.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Skene by specifically providing forming the reference stream with a non-uniform bit pattern, as taught by Ono, for the purpose of giving a graphical break between the start of data transmission.

Regarding claim 27, Skene discloses everything as applied above for claim 20. However, Skene fails to disclose forming the reference stream with a data stream independent of the first serial data stream.

In a similar field of endeavor, Ono discloses a driving control apparatus and driving control method. In addition, Ono discloses inserting start bits, which reads on claimed reference data stream; constituted by an H and an L level before the data being transmitted for effect (claimed first serial data stream), as disclosed at column 5, line 67 and column 6, lines 1-2 and 8-9. Because the start bits will always be comprised of an H level and an L level, this reads on claimed forming the reference stream with a data stream independent of the first serial data stream.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Skene by specifically providing forming the reference stream with a data stream independent of the first serial data stream, as

taught by Ono, for the purpose of signaling the start of the data being transmitted for effect.

22. Claim 31 is rejected under 35 U.S.C. 103(a) as being unpatentable over Skene in view of Hepworth as applied above for claim 28 and further in view of Barbour.

Regarding claim 31, Skene and Hepworth disclose everything as applied above for claim 28. The examiner maintains that it was well known in the art to provide a print head retrieving a first data stream from a print head memory, as taught by Barbour.

In a similar field of endeavor, Barbour discloses a system and method for controlling internal operations of a processor of an inkjet printhead. In addition, Barbour discloses a processor and various controllers within a printhead that may communicate with a memory in the printhead and Barbour discloses the memory holding sensor readings that the processor uses to make decisions, as disclosed at column 5, lines 17-20 and column 8, lines 40-50 and 57-59, which reads on claimed print head receives a first data stream from a print head memory. Thus it can be seen reasonable to one of ordinary skill in the art for the processor to take readings from the memory rather than directly from the sensors. Barbour also discloses the processor communicating with a main memory in a bi-directional manner, as disclosed at lines 40-45.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Skene and Hepworth by specifically providing a print head retrieving a first data stream from a print head memory, as taught by Barbour, for the purpose of processing the data before sending it out to the main controller.

The amendment specifying a data stream to be serial should not make a

difference. Serial and parallel communication are both well known. Serial/parallel conversion has been taught to be well known.

23. Claims 38-39 & 41-42 are rejected under 35 U.S.C. 103(a) as being unpatentable over Skene in view of Hepworth and further in view of Barbour et al. (US 6476928), hereinafter referred to as Barbour.

Regarding claim 38, claim 38 is rejected based on reasoning applied above for claims 1 & 4. It is well known for a print head to be used in a printing apparatus. The parity bit is inserted into the list of bits being communicated in the claimed first data stream in the register, as disclosed above. In order for the received data stream to be validated, the parity code must be correct, which reads on claimed upon receiving a data stream, can validate the received data stream if the received data stream comprises the transmit data stream with the inserted reference data stream. Transmit data stream and received data stream are equivalent and equal the first data stream plus the reference data stream. However, Skene fails to disclose inserting a reference data stream comprising a reference pattern into the first data stream at a reference location after the first data stream has been taken from a memory. It was previously disclosed how the data may be serially and synchronously transmitted in accordance with a clock signal (synchronously and serially transmit the transmit data stream to the host at a control signal clock frequency). However, the examiner maintains that it was well known in the art to provide inserting a reference data stream into the first data stream after the first data stream has been taken from a memory, as taught by Hepworth.

In a similar field of endeavor, Hepworth discloses an asynchronous communication interface adaptor. In addition, Hepworth discloses that when the data is ready to be transmitted, the information in the data register, which reads on claimed memory; is sent to the transmit shift register and inserted are a start bit and a trailing stop bit or bits and a parity may be included, which reads on claimed inserting a reference data stream into the first data stream after the first data stream has been taken from a memory and also may read upon inserting a reference data stream comprising a reference pattern, as disclosed in column 7, lines 23-30. In addition, Hepworth shows that a reference data stream is inserted at a reference location. Col. 7, lines 23-30 disclose the start bit leading, the stop bit or bits trailing, and parity occurring between the last data bit and first stop bit.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Skene by specifically providing Skene fails to disclose inserting a reference data stream comprising a reference pattern into the first data stream at a reference location after the first data stream has been taken from a memory, as taught by Hepworth, for the purpose of adding control and robustness to a serial data stream.

In addition, the examiner maintains that it was well known in the art to provide a printhead comprising a data stream module adapted to retrieve the first data stream from the memory and to transmit the data stream to the host, as taught by Barbour.

In a similar field of endeavor, Barbour discloses a system and method for controlling internal operations of a processor of an inkjet printhead. In addition, Barbour

discloses a processor and various controllers within a printhead that may communicate with a memory in the printhead and Barbour discloses the memory holding sensor readings that the processor uses to make decisions, as disclosed at column 5, lines 17-20 and column 8, lines 40-50 and 57-59, which reads on claimed print head receives a first data stream from a print head memory. Thus it can be seen reasonable for one of ordinary skill in the art for the processor to take readings from the memory rather than directly from the sensors. Barbour also discloses the processor communicating with a main memory in a bi-directional manner, as disclosed at lines 40-45, which reads on claimed transmit the data stream to the host.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Skene and Hepworth by specifically providing a print head retrieving a first data stream from a print head memory, as taught by Barbour, for the purpose of processing the data before sending it out to the main controller.

A "data stream module" is simply a delineation for providing a specified function. Thus, by performing the functions disclosed above and recited in the claim, data stream module is read upon.

Regarding claim 39, Skene, Hepworth, and Barbour disclose everything as applied above for claim 38. Hepworth disclosed above that when the data is ready to be transmitted, the information in the data register, which reads on claimed memory; is sent to the transmit shift register, which reads on claimed data stream register; and inserted are a start bit and a trailing stop bit or bits and a parity may be included, which reads on claimed data stream module comprising a data stream register adapted to

insert the reference data stream.

Regarding claim 41, inherits from claim 38 and claim 41 is rejected upon the reasoning provided in claim 5.

Regarding claim 42, inherits from claim 41 and claim 42 is rejected upon the reasoning provided in claim 6.

24. Claims 40 & 43 are rejected under 35 U.S.C. 103(a) as being unpatentable over Skene in view of Hepworth in view of Barbour and further in view of Ono.

Regarding claim 40, claim 40 is rejected upon the reasoning provided in claim 9. Bits read on claimed data stream.

Regarding claim 43, claim 43 is rejected upon the reasoning provided in claim 8. Bits read on claimed data stream.

Response to Arguments

25. Applicant's arguments filed 3/17/2008 have been fully considered but they are not persuasive.

Due to the large volume of the remarks with regard to a large volume of claims, the applicant's arguments have been attempted to have been addressed at least once. Where an argument is similar with respect to numerous claims, the examiner notes that a response to an argument with respect to one similar claim may stand as a response to arguments with respect to other claim(s).

Regarding the newly amended claim 1 and claims providing similar limitations, the applicant proposed that a data word, which the applicant claims is disclosed by

Skene, is not the same a claimed data stream. However, a stream of data is not length-specific so as to preclude the transmission of a "data word" from reading upon a stream of data, or data stream.

The applicant also proposes that the use of parity bits by Skene does not read on a reference data stream inserted into the first data stream at a reference location. Claim 1 claimed inserting a reference data stream into the first data stream and validating the first data stream based on the reference data stream. The parity bit is sent along with other data from the inkjet cartridge memory (such as information supplied from lines 20a in fig. 2) in order to determine if there might have been a short or error in the transmission of data. Since the parity bit is transmitted along with data (col. 2, lines 7-8) (the transmission of the various stream of data altogether as a data stream, as well as the components being streams of data (with respect to the parity component and the non-parity data component)), it is thus, inserted into the first data stream (the data without the parity bit). The parity bit is a stream of data, as well, and may read upon claimed reference data stream. The parity as a reference to check if there were any errors in the data (first data stream) part, which also reads on claimed validating the first data stream based on the reference data stream.

The applicant also proposes that Hepworth does not teach synchronous communication because the title of Hepworth's invention is asynchronous communication interface adaptor. The examiner understands how this could be confusing, and thus, has attempted to remove the word "asynchronous" from the discussion of Hepworth invention with respect to the claims. This does not alter the

grounds of rejection in anyway, but serves to prevent detraction from the core relevance of Hepworth. Nonetheless, however, calling the whole patent as asynchronous does not preclude the interpretation of a relevant part to be synchronous. The applicant proposes that the by definition, synchronous communication requires the transmission of a clock signal along with the data signal, and that by definition, the only clock signal that could possibly be considered in the application of synchronous communication is that of an externally generated and transmitted clock. However, the examiner respectfully disagrees that synchronous communication only holds one possible interpretation. Nevertheless, as disclosed in the discussion for claim 1, the data is shifted by a clock signal onto a transmit data line for transmission. Thus, the transmission (communication) onto the transmit data line is synchronized with a clock signal, thus reading on synchronously communicating. Even considering the externally-generated and transmitted clock signal proposal, Hepworth discloses in fig. 1 (128), claim 3 and col. 3, lines 31-33 an input transmit clock (external transmitter clock input) from which the synchronization is derived.

In addition, the applicant also respectfully proposes that the combination of Skene and Hepworth are devoid of possible motivation to combine because the technologies are not related. The examiner respectfully disagrees. Hepworth discloses circuitry for communication relevant to systems such as a printer (col. 1, lines 23-29), as does Skene. In addition, the applicant proposes that Skene does not disclose a data stream and that that would render the combination of Skene and Hepworth inoperable. However, the examiner respectfully disagrees. As discussed previously, the

transmission of data represents a data stream. The bits transmitted by Skene could be shifted onto the transmit data line of Hepworth and transmitted. Skene provides communication in parallel form and Hepworth provides parallel to serial and back to parallel again conversion. It would be natural and obvious to combine the two segments together. The bits could still be accessed from the memory of Skene, converted and transported to the controller with the combination of Hepworth, which allows for bidirectional communication, such as between the controller and memory of Skene and vice-versa.

Regarding claim 7 and claims providing similar limitations, the applicant proposes the references do not teach or suggest "inserting a reference data stream into the data stream, wherein the data stream comprises a bit width of at least two adjacent bits." However, this proposal argues limitations not found in the claims. Claim 7 states: "The method of claim 5, wherein the start bits, the sync bits and the stop bits have at least two bits of different voltage values." Claim 5 refers to at least one of a plurality of start bits, a plurality of sync bits, and a plurality of stop bits. Being dependent from claim 5, "the start bits, the synch bits, and the stop bits" of claim 7 thus refer to the at least one of a plurality of start bits, a plurality of sync bits, and a plurality of stop bits mentioned in claim 5, which have been provided for by the disclosure of a "start bit" constituted by two bits, as disclosed by Ono. The disclosures goes on to discuss the two bits (at least two bits) of the "start bit", consisting of an H Level and an L level, which represent two different voltage values. The limitations of claim 7 are specifically

addressed in its provided discussion, and the examiner respectfully maintains the rejection.

Regarding the discussion under the section regarding claims 8-9, 26-27, & 36-37, the proposals of deficiency mentioned under this section do not directly relate to the specific limitations of the mentioned claims. Rather, they propose inadequacies due to amendments or limitations due to dependency. In addition, the only arguments directly specific to particular claims are hidden arguments in regard to independent claims 20 & 28, which are not even mentioned in the section heading.

Regarding claim 38, the examiner notes that no particular statement declared that "the examiner conceded that Skene fails to disclose inserting a reference data stream into the first data stream after the first data stream has been taken from a memory." This is incorrect. The applicant has taken the examiner's words out of context and by doing so, has skewed the interpretation of the discussion regarding claim 38. The examiner maintained that it was well known in the art to provide "provide a printhead comprising a data stream module adapted to retrieve the first data stream from the memory and to transmit the data stream to the host," and accordingly, it would have been obvious to have that limitation within the combination of Skene and Hepworth.

In addition, the applicant proposes that a parity bit is not a reference pattern. However, the examiner respectfully disagrees. A parity bit may represent a concrete, repeatable, and recognizable pattern against a background of other information. In addition, the parity may represent a reference pattern with respect to an even or odd

parity pattern. Even considering the applicant's proposal, en arguendo, numerous multiple recognizable inserts have been disclosed throughout the office action, including stop bits and start bits.

Although the substance of the applicant's arguments is felt to have been addressed, many of the arguments may be rendered moot by the necessitation for new grounds of rejection due to amendments to the claims.

Regarding the applicant's provided personal account of the first office action, the examiner notes that the actual office action should provide the substance and meaning of the discussions of the claims provided from the examiner. The applicant is welcome to provide his or her narration of the office action; however, as some interpretation by the applicant may prove to be false, no particularly strong merit should be accorded to the applicant's assertion of what the examiner meant, or "said;" even, or especially when, the personal interpretations provided by the applicant are not individually addressed.

The discussions provided are in response to arguments of substantiative nature that have been provided with at least some attempt of support or effort at providing evidence. With regard to recitations of limitations that the applicant proposed were not taught or suggested, but were without associated evidence for the proposals, the applicant is referred to the discussion of the claims provided above.

Conclusion

26. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP

§ 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to WILLIAM C. STOREY whose telephone number is (571)270-3576. The examiner can normally be reached on Monday - Friday Eastern Standard Time.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, King Y. Poon can be reached on (571) 272-7440. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/William C Storey/
Examiner, Art Unit 2625

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